Application No.: 09/859,659 Attorney Docket No.: EMC2-090PUS
Reply to Office Action of November 6, 2003

REMARKS/ARGUMENTS

The above-identified patent application has been amended and re-consideration and re-examination are hereby requested.

Referring to the claims, the claims point out that there is a pair of i***ndependent*** controller sections, one of such sections being a primary section and the other one of the sections being a secondary section, both such sections being configured to implement identical control logic ***in controlling the transfer of such data*** *between a first port connected to the pair of controller sections* and a write data port. Thus, the claim points out that there is a first port connected to ***a pair*** of ***independent controller*** sections. Richter does not describe *a first port connected to the pair of independent controller sections,* both such sections being configured to implement identical control logic ***in controlling the transfer of such data*** *between a first port connected to the pair of independent controller sections* and a write data port *as claimed.*

The Examiner states that: "The examiner is reading the parity checkers as sections of a controller, where the controller includes control 120 and two parity checkers 127 and 128. The claimed controller is an obviously inclusion of the two parity checkers and the controller into a single unit." Thus statement is not understood because the applicant is claiming a pair of controllers (referred to in the claim as a pair of controller sections); the applicant is not claiming a single controller. Further, the claim points outs that the pair of controllers sections is configured to implement identical control logic ***in controlling the transfer of such data*** *between a first port connected to the pair of controller sections* and a write data port. It is noted that a parity checker does not control the transfer of data. Thus, the Examiner does recognize that Richter has only a single controller 120 and ***not a pair of independent controller sections*** configured to implement identical control logic ***in controlling the transfer of such data*** *between a first port connected to the pair of independent controller sections* and a write data port.

Claim 9 further points out that each one of the pair of independent controller sections

includes a first parity ***generator***. As pointed out by the Examiner, Richter has a pair of parity ***checkers*** 127, 128. The claim then points out that there is a checker, comprising: a second ***parity generator*** for generating a parity bit from the digital word and for passing there-through to an address/control port either: the parity bit generated by the second parity generator ***or, an inverted parity bit of the parity bit generated by the second parity*** bit generator, selectively in accordance with: whether the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the primary section and the digital word generated by the secondary section are the same or different.

The use of "***an inverted parity bit of the parity bit generated by the second parity***" as claimed, is not shown in Richter or Cloonan taken either singly or in combination.

Claim 10 points out that the memory in the system recited in claim 9 memory is configured to inhibit storage of data at the data port in the memory if either: ***the inverted parity bit of the inverter is passed*** through ***a selector*** to the address/control port because either the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are different; or the digital word generated by the primary section and the digital word generated by the secondary section are different. Such is not shown in Richter or Cloonan taken either singly or in combination. Applicant respectfully requests that the Examiner identify the "selector" in the cited art.

Claim 11 points out that ***each one of the pair of*** independent ***controller sections***, comprises: a first parity ***generator*** coupled to the first port for generating a parity bit for an address/control digital word, such digital word comprising the address/control portion associated with the data at such first port. The claim includes a checker, comprising: a second parity ***generator*** for generating a parity bit from the digital word and for passing there-through to an address/control port either: the parity bit generated by the second parity checker; or, the ***inverted parity bit of an inverter***, selectively in accordance with: whether the parity bit generated by the first parity generator in the primary section and the parity bit

generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the primary section and the digital word generated by the secondary section are the same or different. Such is not shown in Richter or Cloonan taken either singly or in combination. Applicant respectfully requests that the Examiner identify the "inverter" in the cited art.

Claim 12 points out that the memory of claim 11 is configured to inhibit storage of data at the data port in the memory if either: ***the inverted parity bit of the inverter*** is passed through a ***selector*** to the address/control port because either the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are different; or the digital word generated by the primary section and the digital word generated by the secondary section are different Such is not shown in Richter or Cloonan taken either singly or in combination.

Claim 13 points out that ***each one*** of the pair of independent controller sections, comprises: a first parity ***generator*** coupled to the first port for generating a parity bit for an address/control digital word, such digital word comprising the address/control portion associated with the data at such first port. The claim also points out that there is a checker, comprising: (a) a second parity ***generator*** for generating a parity bit for the address/control digital word generated by the primary section; (b) ***an inverter*** for inverting the parity bit generated by the second parity bit generator; (c) a ***selector*** for passing there-through to the address/control port either: the parity bit generated by the second parity checker; or, ***an inverted parity bit of the inverter***, selectively in accordance with: whether the parity bit generated by the first parity generator in the primary section and the parity bit generated by the first parity generator of the secondary section are the same, or different, or if the digital word generated by the primary section and the digital word generated by the secondary section are the same or different. Such is not shown in Richter or Cloonan taken either singly or in combination. Applicant respectfully requests that the Examiner identify the "inverter" and the "selector" in the cited art.

Claim 14 points out that the memory of claim 13 is configured to inhibit storage of

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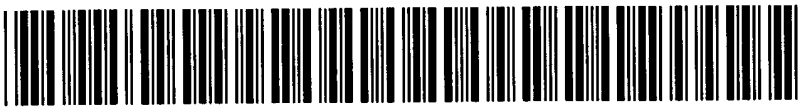

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